REMARKS

Summary of the Office Action

Claims 10-19 are pending.

Claims 10 - 17 have been allowed. However, claims 18 and 19 have been rejected under 35 U.S.C. § 112 as indefinite and as failing to comply with the written description requirement. Further, claim 18 has been rejected under 35 U.S.C. § 102(b) as being anticipated by Desai et al. U.S. Patent No. 5,347,638 ("Desai"). Claim 19 has been rejected under 35 U.S.C. § 103(a) as being obvious over the Desai in view of Miller U.S. Patent No. 5,079,639. Claims 18 and 19 also have been rejected under 35 U.S.C. § 112 as being indefinite.

The Examiner has objected to the Drawings under 37 C.F.R 1.83(a) as not showing the instruction word buffer recited in claim 18.

Applicants' Reply

Applicants appreciate Examiner's allowance of claims 10-17.

Appplicants respectfully traverse the objections to the drawings and the prior art rejections of claims 18 and 19.

37 C.F.R. 1.83(a) Objection to the Drawings

With respect to the objections to the drawings and claim 18, applicants note that FIG. 1 shows a sequence memory 9, which can act as "an instruction word buffer for storing previously used instruction word parts." (See e.g., specification ¶ [0031]). Similarly, "a free row in the instruction word memory 24 or in additional instruction word memory 30" can act as

instruction word buffer. (See e.g., specification ¶ [0032]). Therefore, applicants submit that it is not necessary to further amend the drawings.

Prior Art Rejections of Claims 18 and 19.

With respect to the prior art rejection, applicants' invention relates to arrangement and methods for efficient parallel processing or computing. As summarized in the Abstract of the Specification, the invention relates to methods and arrangements for instruction word generation for controlling of functional units inside a processor. The "execution or controlling" instructions words are generated "in-situ" by expanding or supplementing a "shortened" program word part with "previously used" strings of instruction word parts stored in a reference table. The reference table is indexed (e.g., by row) to allow for quick retrieval of the appropriate string of instruction word parts reused in generating a current "execution" instruction word.

Independent claim 18 is directed to an inventive arrangement, which is configured to generate "execution" instruction words by retrieving an appropriate row of instruction word parts from memory. Applicants note that Desai's apparatus is configured for reloading microinstruction code to an SCI sequencer. Desai does not disclose a buffer for storing previously-used instruction word parts or one which is addressed to recall previously-used instruction word parts [for reuse in generating "new" instruction words for execution], as is required by claim 18. Therefore, claim 18 is patentable over Desai. Further, dependent claim 19 is patentable over the cited prior art for at least the same reason that parent 18 is patentable.

Conclusion

Applicants respectfully submit that this application is now in condition for allowance. If there are any remaining issues to be resolved, applicants respectfully request that the Examiner should kindly contact the undersigned attorney by telephone for resolution.

By: _____

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